CLAIMS

What is claimed is:

1. In a device having a deflection processor (14) developing a deflection processor output signal, a frame drive circuit comprising: a first driver (20) and a second driver (22), said deflection processor output signal being applied to each of said first driver (20) and said second driver (22), each of said first driver (20) and said second driver (22) being selectively operative independently of each other to develop respectively a first coil drive signal (24_OUT) and a second coil drive signal (26_OUT) as a function of said deflection processor output signal, said first coil drive signal (24_OUT) and said second coil drive signal (24_OUT) being applied to a respective one of a first coil half (12) and a second coil half (18) of a frame coil (16).

2. The frame circuit as set forth in Claim 1, wherein the device is a Cathode Ray Tube device comprising a horizontal coil and a vertical coil and the frame coil (16) is one of the horizontal coil or the vertical coil.

3. A frame drive circuit as set forth in Claim 1 wherein each of said first driver (20) and said second driver (22) amplify said deflection processor output signal to develop each respective one of said first coil drive signal (24_OUT) and said second coil drive signal (26_OUT).

4. A frame drive circuit as set forth in Claim 1 wherein each of said first driver (20) and said second driver (22) DC shift said deflection processor output signal to develop each respective one of said first coil drive signal (24_OUT) and said second coil drive signal (26_OUT).

5. A frame drive circuit as set forth in Claim 1 wherein each of said first driver (20) and said second driver (22) include an amplifier (24, 26) having an input (24_IN, 26_IN) and an output (24_OUT, 26_OUT), said input (24_IN, 26_IN) of each amplifier (24, 26) being adapted to receive said deflection processor output signal, said output (24_OUT, 26_OUT) of each amplifier (24, 26) developing an amplified signal for application to a respective one of said first coil half (12) and said second coil half (18).

6. A frame drive circuit as set forth in Claim 1 wherein each of said first driver (20) and said second driver (22) include DC level shifter (28, 30) having an input (28_IN, 30_IN) and an output (28_OUT, 30_OUT), said input (28_IN, 30_IN) of each DC level shifter (28, 30) being adapted to receive said deflection processor output signal, said output

(28_OUT, 30_OUT) of each DC level shifter (28, 30) developing DC level shifted signal for application to a respective one of said first coil half (12) and said second coil half (18).

7. A frame drive circuit of claim 1, wherein the circuit is comprised in an integrated circuit.

8. A method of correcting distortion of an image of a CRT monitor having a deflection processor (14) and a frame coil (16) comprising steps of: selectively developing independently of each other a first coil drive signal (24_OUT) and a second coil drive signal (26_OUT) as a function of a deflection processor output signal developed by said deflection processor; and applying said first coil drive signal (24_OUT) and said second coil drive signal (26_OUT) to a respective one of a first coil half (12) and a second coil half (18) of said frame coil (16).

9. A method as set forth in Claim 6, wherein said developing step includes amplifying said deflection processor output signal to develop each respective one of said first coil drive signal (24_OUT) and said second coil drive signal (26_OUT).

10. A method as set forth in Claim 6 wherein said developing step includes DC level shifting said deflection processor output signal to develop each respective one of said first coil drive signal (24_OUT) and said second coil drive signal (26_OUT).

11. A device comprising: a deflection processor (14) providing a deflection processor output signal; a frame coil (16), said frame coil having a first core half (12) and a second core half (18); a first driver (20) and a second driver (22), said deflection processor output signal being applied to each of said first driver (20) and said second driver (22), each of said first driver (20) and said second driver (22) being selectively operative independently of each other to develop respectively a first coil drive signal (24_OUT) and a second coil drive signal (26_OUT) as a function of said deflection processor output signal, said first coil drive signal (24_OUT) and said second coil drive signal (26_OUT) being applied to a respective one of said first coil half (12) and said second coil half (18).